UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,478	02/27/2004	Gordon Ma	068736.0236	8436

31625 7590 02/24/2006

BAKER BOTTS L.L.P.
PATENT DEPARTMENT
98 SAN JACINTO BLVD., SUITE 1500
AUSTIN, TX 78701-4039

EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,478	MA ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) *24-66* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 9-21* is/are rejected.

7)☒ Claim(s) *2,4-8,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election with traverse of Species I, claims 1-23 in the reply filed on 1/24/06 is acknowledged. The traversal is on the ground(s) that "Applicants hereby elect with traverse". This is not found persuasive because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement.

The requirement is still deemed proper and is therefore made FINAL.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The disclosure is objected to because of the following informalities:

On page 16, par. [0061], line 3, "Fig. 14A" should be changed to "Fig. 11A".

On page 16, par. [0061], line 3, "Fig. 14D to 14I" should be changed to "Fig. 11D to 11I".

Appropriate correction is required.

Claim Objections

4. Claim1-23 are objected to because of the following informalities:

In claim 1, line 3, "first and second insulating layer" should be changed to "first and second insulating layer**s**".

In claims 1-23, line 1, "Semiconductor device" should be changed to "semiconductor device".

In claims 2, line 2, "the first and second via" should be changed to "the first and second via**s**".

In claim 10, line 1, "as claimed in claim 13" should be changed to "as claimed in claim 1".

In claim 15, line 2, "at completely surrounds" should be changed to "at least completely surrounds".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, 12, and 13-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US. 5,151,770) in view of Chang et al (US. 5,767,578).

Regarding claim 1, Inoue (Figs. 4 and 5) discloses a semiconductor device, comprising: a semiconductor substrate 21 (column 4, lines 24-26) having a top and a bottom surface, a first insulating layer 54 and a second insulating layer 55 deposited on the top surface of the substrate, a runner 59 arranged on top of the second insulting layer 55, a backside conductive layer 52 deposited on the bottom surface of the substrate 21, a first via structure 50/55 extending from the bottom surface of the substrate 21 to the top of the first insulating layer 54 between the backside layer 52 and the runner 59, and a second via structure 58 extending from the top of the first insulating layer 54 to the top of the second insulating layer 55 between the first via 50/55 and the runner 59.

Inoue does not disclose that the backside conductive layer 52 is made by metal.

However, Chang (Fig. 11) teaches a semiconductor device having a backside metal layer 104 (column 6, lines 58-61) deposited on the bottom surface of the substrate. Accordingly, it would have been obvious to form the backside conductive layer 52 of Inoue with the metal because the metal is well known and commonly used for providing the electrical contacts.

Regarding claim 3, Inoue (Fig. 4) further discloses that a plurality of second vias 58 are arranged between the first via 50/55 and the runner 59.

Inoue does not disclose that the second via 58 has a smaller footprint than the first via.

However, Chang (Fig. 11) teaches the forming of a first via 124 and a second via 90a formed on the first via 124. The first via 124 needs only be wide enough to establish good electrical paths (column 7, lines 18-19). Accordingly, it would have been obvious to modify the device of Inoue by forming the first via having wider footprint than the second via because the dimension of the second via footprint can be optimized to be wide enough to establish good electrical path, as taught by Inoue (column 7, lines 18-21).

Regarding claim 12, Inoue's Fig. 4 further discloses that the first and second via structures are arranged between a first and second stage 24 and 26 of an integrated device for electromagnetic de-coupling (column 6, lines 20-28).

Regarding claims 14-16, Inoue (Fig. 2) further discloses that the first via is extended in such a way that it at least partly or completely surrounds the first and

second devices 24 and 26, and the first via structure is also extended to form a grid including cells in which certain semiconductor devices 24 and 26 are formed.

Regarding claims 13, 17 and 18, Inoue further discloses that the devices 24 and 26 include amplifiers and an oscillator (column 4, lines 34-37). Therefore, it would have been obvious to form the first device as an active transistor or an input transistor stage including a passive component for forming an oscillator, and the second device as a power transistor output stage for forming amplifiers.

Regarding claims 19 and 21, Inoue (Fig. 40 also discloses that the first device 24 is shielded from the second device 26 and the first device 24 is coupled with the second device 26 through at least one electrical coupling 25 arranged in a first metal layer.

Regarding claim 20, it would have been obvious to form an opening in the second via structure for providing a passageway for the electrical coupling 25 because the location of the electrical coupling can be changed depending upon the requirements for the integrated circuit layout.

7. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue and Chang et al as applied to claim 1 above, and further in view of Jarstad et al (US. 6,472,723).

Regarding claims 9-10, neither Inoue nor Chang disclose that the first via and the second via are filled with tungsten.

However, Jarstad (Fig. 2) teaches a semiconductor device shielded by a shielding structure comprising a plurality of tungsten vias 205 (column 4, lines 46-52). Accordingly, it would have been obvious to fill the first and second vias of Inoue with

tungsten because tungsten is well known and commonly used in the art for providing the electrical conductive plugs.

Regarding claim 11, Jarstad (Fig. 1C) also teaches the forming of the substrate comprising a P+ substrate 101 and P- epitaxial layer 103 for forming an NMOS transistor.

Allowable Subject Matter

8. Claims 2, 4-8 and 22-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 2 and 4-8:

the prior art of record fails to disclose barrier metal layers arranged between the first and second vias, between the runner and the second via, and between the first via and the backside metal layer.

Regarding claims 22-23:

the prior art of record fails to disclose the first via coupling the source region with the backside layer.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
February 17, 2006

PHAT X. CAO
PRIMARY EXAMINER